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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/795,825
Filing Date: March 08, 2004
Appellant(s): AFGHAHI ET AL.

John A. Wiberg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 10/18/06 appealing from the Office action mailed 4/18/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly

affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,343,428 Pilo et al 8-1994

(9) Grounds of Rejection

Claims 1 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Pilo et al.

Note Fig. 1, where the recited "sampling circuit" reads on the combination of inverters 36, 37 and 38 and transmission gates 40 43 and 52; the recited "reference node" reads on either node 101 or 102; and the recited "timing circuit" reads on the (unillustrated) circuitry which outputs the clock signal CLK (note that it activates the sampling circuit prior to measurement of the input signal MUXLAT).

(10) Response to Arguments

Appellant makes two main arguments in the brief, the first argument being that in Pilo et al, node 101 (or, alternatively, node 102) cannot be interpreted as a reference node, and the second argument being that in Pilo et al the timing circuit does not activate the sampling circuit a predetermined interval before measurement of the input signal is initiated. Neither of these arguments is deemed to be persuasive, as will be discussed in detail below.

To support the first main argument, appellant argues that in Fig. 1 of Pilo et al, the node 101 cannot be considered as a reference node because the differential amplifier does not receive a single-ended input signal. This argument is not persuasive because nowhere do any of the claims on appeal require such a single-ended input signal (i.e., appellant is attempting to read a limitation from the specification into the claims).

Moreover, to the extent appellant's node 1021 can be interpreted as a reference node, so too can node 101 of Pilo et al be interpreted as a reference node, because no special definition of the term "reference node" has been provided by appellant in the specification or claims. As such, the term "reference node" is interpreted (using the broadest reasonable interpretation) to simply mean a node having a voltage that is used as a point of reference, i.e., a comparison voltage. As shown in instant Fig. 10, appellant's reference node is simply a capacitive node having a data signal applied thereto, which is exactly what Pilo et al shows in Fig. 1. While appellant is correct in pointing out that appellant's reference voltage is derived from a single-ended input signal whereas the reference voltage of Pilo et al is derived from a differential input signal, the claims are nevertheless still anticipated under 35

U.S.C. 102 (because, as noted above, the claims do not recite a single-ended input signal). Appellant's argument fails because it is an improper attempt to read a limitation from the specification into the claims, as specifically proscribed in section 2145 of the M.P.E.P., see also In re Van Geuns, 26 USPQ2nd 1057 (CAFC 1993).

It is additionally noted that appellant's assertion in the brief at page 5, the last five lines thereof, that the sense amplifier of claim 1 "is not, in fact, a differential amplifier, but conversely, a single-ended amplifier" is also incorrect, i.e., the circuitry illustrated in instant Fig. 10 is clearly a differential amplifier (it is simply a single-ended differential amplifier, a notoriously old and well-known type of differential amplifier). Moreover, appellant even goes on to admit in the brief that instant Fig. 10 includes a differential amplifier (see the last full sentence on page 5 of the brief).

Turning now to appellant's second main argument, it is asserted that in Fig. 1 of Pilo et al "it is precisely the CLK signal...that initiates the measurement of the input signal" and also that "in Pilo, activating the sampling circuit and initiating the measurement of the input signal are one and the same." These interpretations of the operation of Pilo et al's Fig. 1 circuitry are also incorrect, because the activation of

the sampling circuit and the initiation of input signal measurement are not in fact the same. Rather, as noted in the rejection above, the activation of the sampling circuit is performed by the timing circuit, i.e., the circuitry which outputs the clock signal CLK that is applied to the sampling circuit. This clock signal is initially applied to the sampling circuit to activate it, and then once the sampling circuit has been activated, the input signal (MUXLAT, MUXLAT*) is able to pass through to the control terminals of BJTs 26 and 27, and the application of the input signal to transistors 26 and 27 is what allows the measurement of the input signal to take place.

Appellant's assertion in the brief that the measurement of the input signal occurs at the time when the clock signal CLK transitions from low to high is not correct, i.e., the clock transitioning to the high logic state is actually the point when the sampling circuitry is activated.

Finally, appellant argues that "claim 5, and claims 6-8 depending therefrom, are not anticipated by Pilo for at least the reasons set forth above with respect to claim 1." This argument is not persuasive for the same reasons noted above with regard to the arguments against claim 1, i.e., because none of the above-noted arguments has been found to be persuasive, this final argument is also not persuasive.

For the above-noted reasons, none of appellant's arguments is persuasive for overcoming the rejection under 35 U.S.C. 102(b) based on Pilo et al, and it is therefore believed that the rejections should be sustained.

Respectfully submitted,

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